WHAT IS CLAIMED IS:

1. A method for manufacturing a bit line contact structure of a semiconductor memory, said method comprising steps of:

providing a semiconductor substrate;

forming a plurality of gates on the surface of said substrate;

applying a first insulating layer to cover said surface of said substrate and said gates;

selectively forming a plurality of gate contact windows at the locations of said gates;

selectively forming bit line contact windows in said first insulating layer, said bit line contact windows contacting said substrate; and

filling said gate contact windows and said bit line contact windows with a conductive layer.

2. The method as claimed in Claim 1, wherein said semiconductor substrate comprises silicon.

3. The method as claimed in Claim 1, wherein said first insulating layer comprises BPSG, and said method further comprising a step of forming a silicon nitride layer to cover said surface of said substrate and said gates before applying the first insulating

layer.

4. The method as claimed in Claim 1, further comprising a step of performing planarization to expose the upper surfaces of the gates after applying the first insulating layer.

5. The method as claimed in Claim 1, wherein the formation of the gate contact windows and the bit line contact windows mainly uses etching.

6. The method as claimed in Claim 1, wherein the conductive layer comprises W.

7. The method as claimed in Claim 1, wherein the conductive layer further comprises TiN/Ti lying under the W.

8. The method as claimed in Claim 1, further comprising steps of:

forming a second insulating layer of a predetermined pattern on the resultant structure after the filling step, wherein the conductive layer is exposed; and

forming a metal layer on the exposed conductive layer.

9. The method as claimed in Claim 8, wherein the second insulating layer comprises TEOS.

10. The method as claimed in Claim 8, wherein the metal layer comprises W.

11. The method as claimed in Claim 10, wherein the metal layer further comprises a TiN/Ti layer lying under the W.

12. A method for manufacturing a bit line contact structure of a semiconductor

memory, said method comprising steps of:

providing a semiconductor substrate;

forming a plurality of gates on the surface of said substrate;

applying a first insulating layer to cover said surface of said substrate and said gates;

performing planarization to expose the upper surfaces of the gates;

selectively forming a plurality of gate contact windows at the locations of the upper surfaces of said gates;

selectively forming bit line contact windows in said first insulating layer, said bit line contact windows contacting said substrate;

filling said gate contact windows and said bit line contact windows with a conductive layer;

forming a second insulating layer of a predetermined pattern on the resultant structure, wherein the conductive layer is exposed; and

forming a metal layer on the exposed conductive layer.

13. The method as claimed in Claim 12, wherein said semiconductor substrate comprises silicon.

14. The method as claimed in Claim 12, wherein said first insulating layer comprises BPSG, and said method further comprising a step of forming a silicon nitride layer to

cover said surface of said substrate and said gates before applying the first insulating layer.

15. The method as claimed in Claim 12, wherein the formation of the gate contact windows and the bit line contact windows mainly uses etching.

16. The method as claimed in Claim 12, wherein the conductive layer comprises W.

17. The method as claimed in Claim 16, wherein the conductive layer further comprises a TiN/Ti layer lying under the W.

18. The method as claimed in Claim 12, wherein the second insulating layer comprises TEOS.

19. The method as claimed in Claim 12, wherein the metal layer comprises W.

20. The method as claimed in Claim 19, wherein the metal layer further comprises a TiN/Ti layer lying under the W.